A Merged Interleaved Flyback PFC Converter with Active Clamp and ZVZCS

Mehdi Alimadadi, William Dunford

Department of Electrical and Computer Engineering
University of British Columbia (UBC), Vancouver, Canada

Abstract—The design and analysis of a compact flyback AC to DC power supply is described and simulation results are presented. Of particular interest is merging two interleaved power converters such that the main switch in one converter behaves as the clamp switch of the other while ripple cancellation is accomplished. Also, PFC and ZVZCS are achieved with no extra components. Using these approaches, the total number of active and passive components used and consequently the associated power loss, complexity and cost is reduced, which makes the design appealable for low-power high-volume applications. The proposed circuit converts 110VAC to 230VDC at 2.2A load current with an overall simulated efficiency of around 93%.

Keywords—Merged, interleaved, flyback, PFC, active clamp, ZVZCS.

I. INTRODUCTION

To reduce the weight and size of a power converter, it is desired to use a high switching frequency while it has been reported that low frequency isolated converters have better efficiencies [1]. Lower efficiency at higher frequencies is mainly due to increased switching losses that can be compensated using zero voltage/current switching techniques [2].

In an effort to increase conversion efficiency, [3] proposes an AC to DC converter based on flyback topology that recovers the surge energy generated by parasitic inductances to the output side of the isolation transformer. Additional circuitry is used to achieve zero voltage switching (ZVS) during turn on, and voltage clamping during turn off, of the main switch.

In this paper a merged interleaved flyback power factor corrected (PFC) converter with active clamp and zero-voltage zero-current switching (ZVZCS) is introduced. The single-stage conversion proposed here has high power factor, improved efficiency and simple structure with very low number of parts used, which reduces manufacturing cost. Because of these advantages, this converter is recommended for low-power high-volume applications.

Major features of this design are:
- Reduced the total number of components used by merging two parallel power converters and by utilizing single-stage PFC approach.
- Reduced the size of input and output filter components by increasing (constant) switching frequency and by interleaving phases.
- Increased power rating by paralleling phases (not paralleling switches).
- Increased converter output voltage by putting secondary side of the isolation transformers in series (lowered transformer turns ratio).
- Suppressed unwanted voltage surge and oscillations across switches using non-dissipative active clamping without using auxiliary circuitry.
- ZVZCS operation without using auxiliary circuitry.
- PFC functionality without using extra control and current sensing circuitry.

II. CIRCUIT DESIGN

A. Flyback converters with active clamp and ZVZCS

A conventional flyback converter is shown in Figure 1 using solid lines. It is an isolated topology that is derived from the non-isolated buck-boost configuration. When the main switch $S_1$ is turned on, current builds up in the magnetizing inductance $L_{m1}$ of the isolation transformer. The transformer winding polarity is set so that a positive output voltage is obtained. Because of the transformer winding polarity, output diode $D_1$ becomes reversed biased. As such, current does not flow simultaneously in both windings of a flyback transformer, as opposed to the forward topology where current flows simultaneously in both windings and need a demagnetizing winding. The transformer polarity convention used here is: if current flows into the dotted terminal of the primary winding, current will flow out of the dotted terminal of the secondary winding.

When switch $S_1$ turns off, energy stored in $L_{m1}$ (core of the transformer) causes current to flow in the secondary winding through diode $D_1$. As the average voltage applied to the windings should be zero (volt-second balance), ideally the output voltage is given by [4]:

$$\frac{V_{out}}{V_{in}} = \frac{N_{s1}}{N_{p1}} \frac{D}{1-D}$$

(1)

where $D$, $N_{p1}$ and $N_{s1}$ are duty ratio of the switch $S_1$, number of turns of the transformer primary and secondary windings, respectively. The voltage across $S_1$ during turn off is given by (2) which reveals that voltage across main switch is not constant and would be higher at higher duty cycles.

$$V_{s1} = \frac{V_a}{1-D}$$

(2)
To provide for energy storage capability, the isolation transformer must have an air gap. Because of the air gap, the remnant flux density is essentially zero and the relationship between flux density and magnetic field intensity of the core becomes essentially linear [4].

The conventional flyback converter suffers from overvoltage and ringing at the main switch drain terminal at the beginning of turn off interval. This is because as the main switch turns off, current in the transformer’s leakage inductance \( L_{lk1} \) is disrupted and also energy stored in inductor \( L_{lk1} \) can resonate with capacitor \( C_{eq} \). Here, \( C_{eq} \) represents the equivalent capacitance seen between drain-source terminals of \( S_1 \).

Adding a dissipative snubber across the primary winding of the transformer alleviates the problem by clamping the peak of the surging/ringing voltage to a safe level within transistor’s peak voltage rating but it decreases the converter’s overall efficiency.

Another solution is to use a configuration known as two-transistor topology [4]. One extra transistor and two extra diodes are added to the circuit which increases the component count. The voltage rating of the switches is halved as there are effectively put in series.

A third solution is to add an active clamp circuitry (doted lines in Figure 1) which effectively prevents voltage surge/ringing at the main switch drain terminal by providing an auxiliary path for the current in \( L_{lk1} \).

When the main switch \( S_1 \) is turned off, due to the blanking time introduced to provide for the delay needed for ZVS operation, clamp switch \( S_2 \) is not turned on immediately. Current in \( L_{lk1} \) finds its path through body diode of \( S_2 \), causing one diode voltage drop across it. As current in \( L_{lk1} \) charges up the clamp capacitor \( C_{eq} \), it decays and eventually would change direction. The window of opportunity to turn on \( S_2 \) with a small voltage across it (effectively ZVS operation) is when the body diode of \( S_2 \) is conducting (i.e. current in \( S_2 \) is reversed).

Similarly, when \( S_2 \) is turned off, due to the blanking time, \( S_1 \) is not turned on immediately. During this blanking time, reversed \( L_{lk1} \) current finds its way through the body diode of \( S_1 \). As the reversed \( L_{lk1} \) current tries to return charge back to the input supply, it decays and eventually would change direction to charge \( C_{eq} \). When the body diode of \( S_1 \) is conducting, \( S_1 \) can effectively be turned on with ZVS.

Since the leakage inductance of the transformer is utilized as the inductor in an \( LC \) resonator, it has to have a reasonable value to ensure proper operation of the circuit. Leakage inductance increases with loose coupling between primary and secondary windings [5].

The active clamp circuitry, limits the peak voltage applied to the switches, however, the circulating energy between the leakage inductance and the capacitors reduces the overall efficiency. Active clamp circuits have also been used in more complex converter topologies such as full-bridge isolated current-fed converters [6] and soft switching isolated sepic converters [7].

The above discussion was about lossless turn on switching. At turn off, because of the inductances in the circuit, currents in the switches are lagging and switches turn off before their currents reach zero. To employ zero current switching (ZCS) at turn off, small capacitors are added across switches. The disrupted current in the switches will charge up those parallel capacitors [8]. During blanking time before turning switches on, inductor current would remove charge out of those parallel capacitors and transfer it to the load (i.e. switches are turned on with ZVS). This practice will effectively utilize drain-source parasitic capacitance of the MOSFETs.

### B. Merging interleaved converters

Recent trend in power supply design is towards lower voltage and higher current ratings. It has been known that paralleling multi phase converters in general, has many advantages over using one converter with higher power capability. Benefits are: standardization of power modules, system reliability due to redundancy, load sharing and distributed heat generation for better thermal management, to name a few. On the other hand, phase interleaving has the added benefit of increased ripple frequency of the input current and output voltage. Gating signals of separate parallel converters are shifted so that maximum ripple cancellation is achieved. Interleaved converters have faster transient response due to smaller inductances in the circuit and have smaller filter capacitance due to ripple cancellation.
In the proposed design here, to reduce the total number of components used, two parallel flyback converters are merged as shown in Figure 2. Gating signals to the switches have the same duty ratio and are shifted by 180 degrees. Here, the combination of $S_2$ and $C_c$ behaves as the clamp circuitry for a converter consisting of $S_1$ and $T_1$ when $S_1$ is off. Similarly, the combination of $S_2$ and $C_c$ behaves as the clamp circuitry for the converter consisting of $S_2$ and $T_2$ when $S_2$ is off. Thus the proposed circuit is symmetric and both switches operate at similar conditions.

### III. CIRCUIT OPERATION

The following assumptions are used in the analysis of the proposed converter:

- Ideal semiconductors are used.
- Resistive and core losses of the inductors and isolation transformers are negligible.
- Lumped leakage inductances, consisting of primary and reflected secondary leakage inductances, are shown at the primary of isolation transformers.
- Magnetizing inductances are very big.
- Ripple voltage across the capacitor $C_c$ and output capacitors is negligible.

Here, a switching cycle consists of two symmetric half cycles. The second half cycle, repeats the first half cycle in the opposite sense.

#### A. Idealized timing diagram

The idealized timing diagram of the proposed converter of Figure 2 is shown in Figure 3. Waveforms are not to scale. There are four time intervals:

- **Interval 1:** $S_1$ is on and $S_2$ is off. Current in $L_{dl}$ and $L_{m1}$ is increasing. Energy is being stored in $T_1$ core. Current in $L_{dl}$ is decreasing while charging up $C_c$.
- **Interval 2:** Both switches are off (blanking time). Current in $L_{dl}$ starts to decrease while charging $C_{c1}$. Because of the current and voltage polarity shown, current in $L_{m1}$ continues to increase negatively while discharging $C_{c1}$.
- **Interval 3:** $S_1$ is off and $S_2$ is on. Current in $L_{dl}$ and $L_{m2}$ is increasing. Energy is being stored in $T_2$ core. Current in $L_{dl}$ is decreasing while charging up $C_c$.
- **Interval 4:** Both switches are off. Current in $L_{dl}$ starts to decrease while charging $C_{c2}$ and current in $L_{m2}$ continues to increase negatively while discharging $C_{c2}$.

#### B. Idealized current path diagram

The idealized current path diagram of the proposed converter of Figure 2 is shown in Figure 4. Referring to timing diagram of Figure 3, there are four time intervals:

- **Interval 1:** Energy is being stored in $L_{dl}$ and $L_{m1}$ (core of $T_1$). The energy will be used during next Interval 3. While energy that was previously stored in $L_{m2}$ is being clamped, energy that was previously stored in $L_{m1}$ (core of $T_1$), is being transferred to the output stage.
- **Interval 2:** No energy is being transferred to output.
- **Interval 3:** Energy is being stored in $L_{dl}$ and $L_{m2}$. The energy will be used during next Interval 1.

While energy that was previously stored in $L_{dl}$ is being clamped, energy that was previously stored in $L_{m1}$, is being transferred to the output stage.

### IV. SIMULATION RESULTS

The complete circuit diagram shown in Figure 5 is simulated using PSIM [9] to provide voltage and current waveforms and efficiency values. Those simulation results can be used to evaluate component stress under different circumstances that would translate into cost, size and efficiency [10].

Simulations are done using the following assumptions:

- Duty ratio adjusted by an output voltage feedback proportional-integrator (PI) control loop.
- Diode voltage drop of one volt.
- MOSFET on resistance of 25m Ω.
- Isolation transformer turns ratio of $N_p/N_s = 1/2$.
- Resistances of the windings are negligible.
- Other component values as noted on the schematic diagram of Figure 5.

In the circuit of Figure 2, because of the extra current path provided by the clamp circuitry, current in the leakage inductance of the isolation transformers can go negative. The circuit of Figure 5 uses a diode bridge at the input which would prevent negative current to the converter. As there might be operating conditions that charge needs to be returned to the input supply (bus pumping) and a rectifier bridge restricts that action, a capacitor needs to be added after the input diode bridge to provide a path for the negative current.

#### A. Waveforms of points of interest

Simulated voltage and current waveforms are provided in Figure 6 at the peak of input voltage with $V_{out} = 230V$ and $I_{out} = 2.2A$. Waveforms are scaled.

The voltage across $S_1$ also shows that the MOSFET operates with ZVZCS. The applied gating signal goes high while the body diode of the MOSFET is conducting (current through the switch is negative) and when the gating signal goes low, first current though the switch decays and then voltage across the switch increases. Also, it can be seen that the voltage across $S_1$ is well clamped and there is a minimal overshoot or ringing, thus no extra snubber circuitry is needed for the switches.

Figure 6 also shows the input current which is (semi-) sinusoidal and is in phase with the input supply voltage.

#### B. Table and graph of values of interest

As the efficiency of a converter is becoming an important parameter to gauge its performance, the efficiency is not only reported at full load current but also at other load currents such as 25, 50 and 75 percent of the full load. Figure 5 has been simulated at different load currents to provide converter efficiencies presented in Table 1, running at the same conditions as above.

To investigate the effect of changing the input voltage on operation of the converter, Figure 5 was simulated by sweeping $V_{in}$ from 90V to 160V at a constant output...
power of 500W and the results are shown in Figure 7. At low input voltages ($V_{in} < 108V$), duty ratio is saturated to 50% as a higher duty ratio is needed to maintain the output voltage at 230V, thus no control is available. At high input voltages ($V_{in} > 113V$), a lower duty ratio is needed to maintain the output voltage at 230V and thus ZVS operation is not performed and consequently, overall converter efficiency drops. The input operating voltage of 110V is inside the input voltage range that ZVS operation is performed ($108V < V_{in} < 113V$) where also the simulated efficiency is above 90%.

Figure 3. Idealized timing diagram of Figure 2

Figure 4. Idealized current path diagram of Figure 2
V. DISCUSSION

A. Inherent PFC operation

As power supply manufacturers are trying to sell their products in a global market, limiting the input current harmonics to the levels documented in IEC-6000-3-2 is recommended [11] [12]. Traditionally a PFC stage is put before a power converter stage, effectively putting two power stages in series. The two-stage approach has some disadvantages such as overall efficiency drop due to double conversion and higher cost. A single-stage approach merges the two separate power stages together, alleviating the above disadvantages [13].

If a single-stage PFC converter is working in discontinuous conduction mode (DCM), PFC functionality is automatically achieved [14]. Using DCM approach, additional input current sensing and current controller circuitry is not needed which would reduce overall complexity and cost. The complexity comes from the fact that the operating point of the PFC circuitry constantly changes as the instantaneous magnitude of the input AC voltage changes with time during each AC period [15]. Using this approach, current control loop and related stability difficulties are removed and thus only the output voltage has to be sensed and controlled. Operating in DCM also means that the inductor would have larger current swings, resulting in more resistive losses and a bigger filter at the input. This would make the discontinuous mode more appealing for lower power levels.

B. Challenges and limitations

Each output stage of the proposed converter has to use a single diode as shown in Figure 2 because the converter is based on flyback topology. A different type of output stage configuration, such as full diode bridge, creates a different current path that is not compatible with the requirements of flyback topology.

There are also other restrictions regarding the proposed design as follows:

- Because gating signals to the switches have same duty ratio and are shifted by 180 degrees, duty cycle needs to be restricted to a maximum of 50% (40% considering 0.5µs blanking time at 200kHz to provide for the delay needed for ZVS operation).
- Since the proposed converter is based on flyback topology, voltage across switches during turn off is higher than the input voltage, as discussed in Section 2. Because this converter operates at lower than 50% duty ratios, this issue is not as severe as if it was operating at higher duty ratios.

<table>
<thead>
<tr>
<th>$R_{cut}$ (Ω)</th>
<th>$P_{cut}$ (W)</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>106</td>
<td>500</td>
<td>93</td>
</tr>
<tr>
<td>141</td>
<td>375</td>
<td>84</td>
</tr>
<tr>
<td>212</td>
<td>250</td>
<td>74</td>
</tr>
<tr>
<td>424</td>
<td>125</td>
<td>66</td>
</tr>
</tbody>
</table>
• At low duty cycles, both transistors are needed to be on for a shorter amount of time. Thus the time between when one switch is turned off and the other switch is turned on is increased. This will result in turning on a transistor while the window of opportunity for ZVS operation (see Section 2) has long been closed. Thus ZVS operation won’t be achievable at lower duty cycles. Similarly, at low output currents, because a lower current for a shorter amount of time is passing through the body diodes of the switches, the window of opportunity closes quickly and thus ZVS operation won’t be achievable at lower output currents either.

• If complimentary duty cycles were to be used, duty cycle \( D \) would be applied to one individual converter while \((1-D)\) would be applied to the other. As the design is based on flyback topology, according to (2) at \(Ds \) other than 50\%, one switch will see much higher voltage across it compared to the other one. As a result, \( C _ c \) will have a relatively high voltage swing resulting in excessive current through it, which makes this scenario of no use.

• If complimentary duty cycles were to be used, according to (1) at \(Ds \) other than 50\%, each individual converter will have a different output voltage, thus the output stages can not be put in parallel. In this design, since the output stages are put in series, output voltages will add up to provide \( V _ {out} \). As \( D \) varies, \( V _ {out} \) won’t be constant because:

\[
\frac{V _ {out}}{V _ {in}} = \frac{D}{1-D} + \frac{1-D}{D}
\]

and \( V _ {out} \) still can be adjusted. On the other hand, output power won’t be equally shared by the converters and the circuit becomes unbalanced.

• If complimentary duty cycles were to be used, at \(Ds \) other than 50\%, currents passing through the converters are not the same. And potentially, the converter with lower duty cycle/current won’t have ZVS while the converter with higher duty cycle/current would.

• While the converter is connected to the input supply and there is no switching activity (all switches are off), the clamp capacitor \( C _ c \) gets charged to the peak of the supply voltage. Although there are many other circuits reported in the literature with the same drawback such as the one in [3], a circuit that is based on full-bridge configuration does not have this disadvantage.

• The converter can be controlled by a digital controller which can handle complex situations. In that case, the inherent time delay introduced by the controller, needs to be dealt with, else, large overshoots and ringing in the output would occur [16].

VI. CONCLUSIONS

In this paper, a low-power high-frequency isolated AC to DC converter has been proposed and its performance has been studied. Two interleaved flyback converters have been merged and a single-stage PFC approach is used to reduce the total number of components. It was demonstrated by simulation, that the proposed converter has high efficiency inside the input voltage range that ZVS operation is performed.

The proposed converter has a simple structure, which reduces manufacturing cost for low-power high-volume applications. Together with the Tri-port configurations investigated in [1], this is another step in the development of a low cost UPS system.

ACKNOWLEDGMENT

This work has been supported in part by funding from MITACS ACCELERATE research grant.

REFERENCES


