Small Signal Analysis and Controller Design of a Half-Bridge Single-Stage Power Converter

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Abstract—In this paper, a half-bridge single-stage power converter is used as a fundamental study object. The half-bridge single-stage power converter proposed in this thesis has inherent gift of high power factor correction (PFC) even when the PFC inductor operates in discontinuous conduction mode (DCM). It is revealed that if the proposed converter is operating in DCM, it not only inherently has high power factor but also avoids the bulk capacitor from high voltage stress at light loads.

Having decided the operating mode of the converter, the state-space averaged model is used to drive the DC operating point and the small signal model. Then each component of the proposed converter is designed to satisfy the specifications. The output voltage is ensured by Simulink simulations.

Finally, experimental results are used to verify the accuracy of small-signal model wherein the voltage feedback controller is designed to regulate output voltage. The experimental results show good confirm with the analysis and designs.

Keywords—small signal analysis; half-bridge converter; single-stage; DCM

I. INTRODUCTION

There are many of single-stage power converters proposed in [1-5] and related control schemes in [6-10] to achieve both the functions of power factor correction and DC output regulation, with the component count reducing thereby the cost and the volume down, and with the efficiency increasing due to the single-stage structure. To regulate the load varying, the small signal analysis or model depicted by transfer function must be found to design an appropriate controller for compensations of the error between output and reference and the dynamic response. Generally, the state-space averaging method easy to derive transfer functions of power converters is well-known and reliable so that the controller in feedback loop can be designed in accordance with the transfer function from this averaging method.

II. SMALL SIGNAL ANALYSIS OF THE PROPOSED CONVERTER

The half-brie single-stage power converter is shown in Fig. 1. From the principles and operations in this converter, the averaged state equations can be obtained as below

\[ \begin{align*}
C_2 \frac{d \tau_{CB}}{dt} &= \frac{d^2 T_S}{2} \left[ \frac{\tau_{CB} + \tau_S}{L} \left( \frac{2\pi S}{\tau_{CB} - \tau_S} \right) - \left( n(n\tau_{CB} - \tau_O) \right) \right] \\
C_O \frac{d \tau_O}{dt} &= \frac{d^2 T_S}{2} \left[ n (\tau_{CB} - \tau_O) \right] \frac{\tau_O}{R}
\end{align*} \]  

wherein constants A~H are determined by combinations of the circuit operating parameters

\[ \Delta = S^2 + [B + F]S + B \times F - G \times \frac{1}{C_C} \times H \]

In general, the AC gain of the common PWM controller can be illustrated in Fig. 3 and can be expressed as

\[ \frac{\tilde{v}_O(S)}{d_i(S)_{k_i(S)=0}} = \frac{1}{C_O} \times \left[ AS + A \times B + C \times \frac{1}{C_2} \times D \right] \]

\[ \frac{\tilde{v}_O(S)}{\tilde{v}_S(S)_{d_i(S)=0}} = \frac{1}{C_O} \times \left[ C \times \frac{1}{C_2} \times E \right] \]

The used closed-loop control block diagram is illustrated in Fig. 2 wherein the dynamic characteristics will be depicted by the function of \( \tilde{v}_O \) to \( \tilde{v}_C \). Hence, the disturbance components are introduced into the state equations and using Laplace transformation to find the functions as

\[ \frac{\tilde{v}_O(S)}{d_i(S)_{k_i(S)=0}} = \frac{1}{C_O} \times \left[ AS + A \times B + C \times \frac{1}{C_2} \times D \right] \]

\[ \frac{\tilde{v}_O(S)}{\tilde{v}_S(S)_{d_i(S)=0}} = \frac{1}{C_O} \times \left[ C \times \frac{1}{C_2} \times E \right] \]

wherein constants A~H are determined by combinations of the circuit operating parameters and

\[ \Delta = S^2 + [B + F]S + B \times F - G \times \frac{1}{C_C} \times H \]

In general, the AC gain of the common PWM controller can be illustrated in Fig. 3 and can be expressed as

\[ \frac{\tilde{d}_1(S)}{\tilde{v}_C(S)} = \frac{1}{V_M} = k_{PWM} \]

\[ \Delta = S^2 + [B + F]S + B \times F - G \times \frac{1}{C_C} \times H \]
While substituting the circuit parameters listed in TABLE I into (2) and (3), the transfer functions can be rewritten as

$$\frac{\tilde{v}_O(S)}{\tilde{v}_S(S)} \bigg|_{d_1(S)=0} = \frac{88.97}{S^2 + 20.6S + 49}$$

(6)

$$\frac{\tilde{v}_O(S)}{\tilde{d}_S(S)} \bigg|_{d_1(S)=0} = \frac{1.235 \times 10^4 S + 5.854 \times 10^4}{S^2 + 20.6S + 49}$$

(7)

The controller is designed using Pole/Zero elimination method to fill the output regulation in which usually the bandwidth is set as $1/5$~$1/2$ of the switching frequency and the phase margin need to be $45^\circ$ or larger such that a 3-pole/2-zero controller shown in Fig. 4 is used and the corresponding transfer function is

$$G_c = \frac{G_{k}\omega_c}{S} \times \frac{\left(\frac{S}{17.86} + 1\right)\left(\frac{S}{2.744} + 1\right)}{\left(\frac{S}{4.741} + 1\right)\left(\frac{S}{62.831 \times 10^3} + 1\right)}$$

(8)

wherein the respective frequencies related to this 3-pole/2-zero controller and the corresponding element values are as below if $C_1 = 10 \, \mu F$ is set,

\[
\begin{align*}
    f_1 &= \frac{3.666}{2\pi} = 0.58 \text{ Hz} \\
    f_2 &= \frac{6.2831 \times 10^3}{2\pi} = 10 \text{ kHz} \\
    f_3 &= \frac{2.29}{2\pi} = 0.36 \text{ Hz} \\
    f_4 &= \frac{16.5}{2\pi} = 2.62 \text{ Hz}
\end{align*}
\]

(9)

\[
\begin{align*}
    R_1 &= 16.46 \text{ k} \Omega \\
    R_2 &= 27.2 \text{ k} \Omega \\
    R_3 &= 6.06 \text{ k} \Omega \\
    C_1 &= 10 \, \mu F \\
    C_2 &= 0.003 \, \mu F \\
    C_3 &= 10 \, \mu F
\end{align*}
\]

(10)

### III. EXPERIMENTAL RESULTS

To verify the feasibility of the compensated system under the parameters listed in TABLE I, the block diagram is depicted in Fig. 5 using Simulink and the system transfer function is

\[
T_c(S) = \frac{9.954 \times \left(\frac{S}{4.741} + 1\right)}{\left(\frac{S}{17.86} + 1\right)\left(\frac{S}{2.744} + 1\right)} \times \frac{G_{k}\omega_c}{S} \times \frac{\left(\frac{S}{17.86} + 1\right)\left(\frac{S}{2.744} + 1\right)}{\left(\frac{S}{4.741} + 1\right)\left(\frac{S}{62.831 \times 10^3} + 1\right)}
\]

(11)
wherein $G_0\omega_c=8024$ is calculated with above-mentioned parameters. Fig. 6 shows the simulated output voltage is fixed at the required 200V.

<table>
<thead>
<tr>
<th>TABLE I. CIRCUIT DESIGN PARAMETERS</th>
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<tbody>
<tr>
<td>Input voltage $V_S$</td>
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<tr>
<td>Output voltage $V_O$</td>
</tr>
<tr>
<td>Voltage on bulk capacitor $V_{CB}$</td>
</tr>
<tr>
<td>Input inductance $L$</td>
</tr>
<tr>
<td>Output inductance $L_O$</td>
</tr>
<tr>
<td>Duty cycle $d_1$</td>
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<tr>
<td>Switching frequency $f_S$</td>
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<tr>
<td>Bulk capacitances $C_1$, $C_2$</td>
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<tr>
<td>Output capacitance $C_O$</td>
</tr>
<tr>
<td>PWM gain $K_{PWM}$</td>
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<td>Turn ratio $n$</td>
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</table>

The complete system is shown in Fig. 7, including the power stage of half-bridge single-stage power converter, the feedback circuit used to sample the output voltage and generate the error signal for compensation, the designed 3-pole/2-zero controller, the PWM controller such as TL494 from TI herein, the gate driver circuit and the zero-crossing detector used to distinguish the positive-half-cycle and negative-half-cycle of the source voltage. It is noted that the low-side power switch $S_2$ and the free-wheeling diode $D_1$ are switching responsible for positive-half-cycle and the high-side power switch $S_1$ and the free-wheeling diode $D_2$ are switching responsible for negative-half-cycle in the proposed control strategy. The corresponding Bode plot is shown in Fig. 8, wherein the designed phase margin is presented 45° obviously. Experimental results are illustrated in Figs. 9 and 10. Fig. 9 shows the source current can follow that voltage exactly well, therefore the required PFC function is verified. Noted that an AC capacitor which is not shown in the figures will be parallel with the AC source $v_s$ to filter the harmonics in the shown source current so that the actual source current will be profiled a sinusoid as the source voltage. Fig. 10 shows the output responses while the equivalent load varies between the equivalent loads 400$\Omega$ and 1.5k$\Omega$. It is clear that the output voltage can be regulated at designed 200V and the responses satisfy the output regulation. The measured power factor curve and the efficiency curve under various equivalent loads are illustrated in Fig. 11. Fig. 11 depicts that PF and efficiency of the implemented prototype half-bridge single-stage power converter are above 0.96 and 0.85 respectively, and it shows the good performance and the experimental results are consistent with the design specifications.
IV. CONCLUSIONS

The small signal analysis for a half-bridge single-stage power converter is carried out and the controller used for compensation is designed and confirmed with this analysis by simulations and experiments. The output voltage regulation is fulfilled through the design using the proposed small-signal analysis. Experimental results give good conform to the predetermined specifications.

REFERENCES