Digital Primary-Side Sensing Control for Flyback Converters

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Abstract—Primary-side sensing (PSS) technique can be used for the output voltage or current regulation by employing an auxiliary winding. However, the sensed voltage may be corrupted by switching noise due to leakage inductance, winding resistance, and nonlinearity of the magnetic core, therefore the sensed voltage can only achieve limited accuracy. With the advance of power control IC realization technology, more complicated control and estimation algorithms can be realized by using analog, digital, or mixed-signal technologies. This paper introduces a digital control method to make the influence of nonideal factors as low as possible. A key factor for accurate voltage sensing is the determination of sampling instant on the auxiliary winding. A prototype of a DCM DC/DC flyback converter with digital signal processor has been realized to verify the proposed digital PSS scheme.

Index Terms—Primary-side sensing, digital control, flyback.

I. INTRODUCTION

Conventional flyback converters utilize an error amplifier and an opto-coupler to implement the voltage feedback compensation and galvanic isolation. Although Flyback converter topology gets its wide applications in low-power and low-cost isolated switching power supplies due to its low component counts without a secondary output filter inductor, it suffers from the CTR (current transfer ratio) degradation due to temperature rise for low-cost opto-couplers. This makes a constraint on operating temperature for the flyback converter in applications to high power loads. The elimination of the opto-coupler provides significant advantages such as higher power density, cost down, and lower standby power. Therefore, primary-side sensing (PSS) technique, which senses the output voltage from the primary or auxiliary winding of the transformer without using the opto-coupling circuit, becomes an important issue for the development of more sophisticated flyback control ICs.

Another motivation to develop PSS technique is that there is a low frequency pole at 20-30 kHz from the opto-coupler. This pole complicates the feedback loop design and limits the crossover frequency. Recently, in order to get a higher crossover frequency in voltage loop, engineers may implement secondary-side control, which places the controller at the secondary side and transmits the pulse-width-modulation (PWM) signal through a pulse transformer or a high-speed photodetector to eliminate the low frequency pole, but the start-up circuit needs the electrical isolation from the input power [1]. Hence, PSS technique combines the advantages of primary-side control and secondary-side control to become an attractive choice.

The output voltage appears on the primary winding during the power switch off state, therefore the PSS technique can extract the output voltage from the primary side [2]-[5]. The requirement for this method is the implementation of high voltage sensing circuits and suffers from coupling noises due to primary leakage inductance. Another approach is to adopt an additional auxiliary winding to detect the output voltage [6]-[10]. This auxiliary winding can be used for both power supplying and voltage sensing and it provides advantages such as low-voltage IC manufacturing process for the implementation of CMOS controller for cost reduction, better winding mechanism for the reduction of coupling noises, lower standby power consumption using the same IC manufacturing process.

The accuracy of sensing the output voltage indirectly from the auxiliary winding will be influenced by practical factors, such as cross coupling effect, voltage drop across secondary winding, and switching oscillations induced by leakage inductance, magnetization inductance, and the output junction capacitance of the switching device. The PSS error analysis has been developed in [11]. In accordance with the regulatory agencies of the intended market, such as IEC950 in Europe and UL1950 in the U.S., Commercial flyback transformers must provide galvanic isolation between primary and secondary winding. Different approaches can be adopted to meet the required safety regulations. Cores and bobbins are usually selected large enough meet the creepage distance requirement as well as to maintain transformer coupling and reduce leakage inductance. Cross coupling between transformer windings should be attended when we sense the output voltage from the auxiliary winding.

This paper describes PSS technique in section II. And then, the analysis and design of a DCM DC-DC flyback converter are discussed in section III. A prototype of a DCM DC-DC flyback is implemented to verify PSS technique, and the experimental results are shown in section IV. Finally, Section V is the conclusion.

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II. PRIMARY-SIDE SENSING TECHNIQUE

In this paper, the output voltage is sensed from the auxiliary winding of the flyback transformer. The proposed flyback converter with PSS is conceptually shown in Fig. 1. All definitions and equations in this section are based on [11]. The power switch off state can be divided into three intervals  $T_1$, $T_2$, and $T_3$. The definitions of interval $T_1$, $T_2$, and $T_3$ are shown in Fig. 2. All components and parameters in the secondary and auxiliary side converted to the primary side are noted with prime as ‘$\prime$’. For instance, $v_{a} = n v_{a}'$, where $n$ represents the turn ratio from the primary side to the secondary side.

It is recommended to sense the output voltage during interval $T_1$, so the lengths of interval $T_1$, $T_2$, and $T_3$ are necessary to be estimated as

$$T_1 = \frac{L_M i_{p}'}{K_p} \frac{1 + K_p + K_s + K_a}{v_o (1 + K_s + K_a) - K_s v_o' - K_a v_{aux}'}$$  \hspace{1cm} (1)

$$T_2 = \frac{L_M i_p}{K_p} \frac{K_s v_o' + K_p v_o - v_{aux}' (1 + K_s + K_p)}{v_o' (1 + K_s + K_a) - K_s v_o' - K_a v_{aux}'} \left(1 + K_s + K_a\right)$$

$$\frac{v_{aux}'}{v_{aux} + v_{aux}' K_s - K_a v_o'}$$  \hspace{1cm} (2)

$$T_3 = \frac{i_p L_M}{v_o} \frac{(v_{aux}' - v_o')(1 + K_s)}{v_o' v_{aux}' + K_s (v_{aux}' - v_o')}$$.  \hspace{1cm} (3)

where

$$K_s = L_M / L_{iks}, \quad K_a = L_M / L_{ika}, \quad K_p = L_M / L_{ilp}.$$ and

$L_M$: magnetizing inductance
$L_{ilp}$: leakage inductance in the primary winding

When the output voltage is sensed in interval $T_1$ from the auxiliary winding, the voltage on the auxiliary winding is

$$v_{aux} = \frac{K_s N_a}{1 + K_s N_s} \left(v_o + v_D + i_s R_s\right)$$  \hspace{1cm} (4)

where $n_{eff}$ is defined as the effective turns ratio, $v_D$ is the voltage drop of the secondary diode, and $R_s$ is the winding resistance at the secondary side. The system estimates the output voltage from the voltage on the auxiliary winding. The sensing error can be derived as

$$\Delta v = v_{o,est} - v_o = \frac{v_{aux}}{n_{eff}} - v_o$$  \hspace{1cm} (5)

$$= v_D + i_s R_s.$$

The proposed PSS control scheme was implemented by a single-chip DSP controller, the TMS320F2812, to study its feasibility. The control procedure includes three major steps:

(1) sample the sensed voltage from the auxiliary winding. (2)
Calculate duty command \( V_{duty} \) to regulate the output voltage for flyback converters. (3) Set the sampling instant by \( V_{ADC} = V_{delay} + V_{duty} \). The mechanism to set the sampling instant is shown in Fig. 3. The more detailed timing diagram of PSS algorithm in the DSP chip will be mentioned in section IV.

III. ANALYSIS AND DESIGN OF A DCM DC-DC FLYBACK CONVERTER WITH PSS

A. Dynamic model

Although the system is implemented by PSS, the control-to-output transfer function is the same as the conventional flyback converter and is expressed as

\[
\frac{\tilde{y}_o}{d}(s) = \frac{\tilde{v}_m}{\sqrt{K}} \frac{1}{1 + \frac{s}{2RCLC}} \quad \text{with} \quad K = \frac{2LCL}{RCLC}T_s
\]

where \( T_s \) is the switching period. For this prototype, the block diagram is shown in Fig. 4. The dynamic model of digital trailing edge pulse-width-modulation (DPWM) block is obtained from [12] and can be expressed as

\[
\frac{\tilde{d}}{V_{duty}}(s) = \frac{e^{-DT_s}}{V_{tri}}
\]

where \( V_{tri} \) is the peak value of the sawtooth carrier in the DPWM. The exponential term represents a delay factor and can be simplified by the first-order Padé Approximation, so (7) can be expressed as

\[
\frac{\tilde{d}}{V_{duty}}(s) \approx \frac{1 - \frac{1}{2}DT_sS}{V_{tri} + \frac{1}{2}DT_sS}.
\]

In (8), the DPWM is a linear phase system. The feedback path is composed by the transformer and the voltage divider, so the feedback gain \( H \) can be obtained as

\[
H = n_{eff} \frac{R_{ac2}}{R_{ac1} + R_{ac2}}.
\]

For TMS320F2812, sixteen 12-bit ADCs are built-in. When ADCs are used to sample analog signals, the gain \( K_{ADC} \) should be concerned in the control loop, which is expressed as

\[
K_{ADC} = \frac{2^B}{v_r}
\]

where \( B \) is the number of bits of ADCs and \( v_r \) is the input range of ADCs.

B. Digital PI controller

This paper develops the continuous time equivalent model of the digital control loop in Fig. 5, which considers the controller is an analog controller. Because the control-to-output transfer function in DCM flybacks is a first-order system. Then, a PI controller is a good choice and the backward Euler integration method can actually be implemented. We have to determine the loop gain for the block diagram of Fig. 5. The loop gain is given by the cascade connection of all blocks as follows

\[
L(s) = \left( K_p + \frac{K_i}{s} \right) \frac{1 - \frac{1}{2}DT_sS \tilde{v}_o(s)}{V_{tri} + \frac{1}{2}DT_sS} HK_{ADC}. \]

Choose a proper crossover frequency \( f_{cl} \) and phase margin (PM) according to the desired specification. The parameters \( K_p \) and \( K_i \) can be obtained by solving the following equations with an assumption that \( K_i = 2\pi f_{cl} K_p \).

\[
\begin{align*}
|L(j \cdot 2\pi f_{cl})| &= K_p \frac{\tilde{v}_o}{V_{tri}} \frac{1 - \frac{1}{2}DT_sS \tilde{v}_o(s)HK_{ADC}}{2 \pi f_{cl} DT_s} \\
-180 + PM &= -90 - 2 \tan^{-1} \left( 2\pi f_{cl} \frac{K_p}{K_f} \right) \\
& \quad - \tan^{-1} \left( 2\pi f_{cl} \frac{K_p}{K_f} \right)
\end{align*}
\]

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C. Modulating the sampling instant

$V_{\text{delay}}$ is a key parameter for the primary-side sensing technique. In order to sense the output voltage in interval $T_3$, $V_{\text{delay}}$ times $T_{\text{CLK}}$ should be larger than $T_1$ plus $T_2$, where $T_{\text{CLK}}$ is the period of the counter. The ADC will sample the sensed voltage at $V_{\text{delay}} T_{\text{CLK}}$ after the switch turned off. There is a problem that a steady-state error occurs when using a constant $V_{\text{delay}}$ for different loads, which is shown in Fig. 6. This steady-state error is caused by the sensing error according to (5) that the current $i_s$ at the sampling instant changes with different loads. To improve the voltage regulation, a method is to modulate the sampling instant with different loads.

Figure 7 shows the concept of modulating $V_{\text{delay}}$ with different loads.

\[ V_{\text{delay}} = \frac{t_{\text{off}} - \Delta t}{T_{\text{CLK}}} \quad (13) \]

where the interval $t_{\text{off}}$ can be estimated from the magnetizing current $i_M$, so it can be derived as

IV. EXPERIMENTAL RESULTS

To verify primary-side sensing (PSS) technique, a 90 W DCM flyback converter is designed for operation from the 100 V dc line. The nominal output voltage is 19 V, the switching frequency is 50 kHz, the magnetizing inductance is 120 $\mu$H referred to the primary side, the flyback transformer turns ratio $n$ is 2.9, the effective turns ratio $n_{\text{eff}}$ is measured as 1/3, and the output capacitance is 200 $\mu$F.

A. Voltage regulation

First, the voltage regulation results with and without modulating the sampling instant are shown in Fig. 8. The testing point is set from 20 W to 90 W. All results are normalized by 19 V. The voltage regulation with modulating the sampling instant has 1% deviation when the load power is from 20 W to 90 W, and the voltage regulation with constant sampling instant has about 4% deviation. As a result of modulating the sampling instant, the voltage regulation can be improved.

B. Timing diagram of PSS algorithm in the DSP chip

There is one interrupt service routine (ISR) program, which is called ADC_ISR, to implement PSS technique. The ADC interrupt is set to be compared interrupt flag, so ADC_ISR will be triggered when the register $V_{\text{ADC}}$ is equal to the counter. In Fig. 9, the sensed voltage is converted to digital value by ADC first, which costs 0.49 $\mu$s. Then, the digital PI controller calculates the next duty command according to the sensed value and the output voltage command, which costs 0.36 $\mu$s. Finally, a modulating method in (13) is utilized to update the next sampling instant, which costs 0.54 $\mu$s. The total duration of ADC_ISR is 1.39
μs, which is about 7% to the switching period.

C. Load transient response

We test the load transient from 20% to 100% with and without modulating the sampling instant. Figure 10 shows the result with constant sampling instant and Fig. 11 shows the result with modulating sampling instant. It is obvious that there is a steady-state error, 700 mV, in Fig. 10, which is caused by sensing error mentioned before. When the sampling instant is modulated by (13), the steady state error is reduced. Moreover, the modulation of the sampling instant does not affect the dynamic response because the waveforms in Fig. 10 and 11 are similar.

For operating in DCM, the output voltage of flyback converters suffers from the ESR of the output capacitor. To improve this situation, install a small LC filter at the output. Both load transient responses are shown together in Fig. 10 and 11. PSS technique senses the voltage before the LC filter, so the dynamic response of the LC filter does not affect the controller design.

The settling time in both cases is the same as 420 μs. Because of the sampling frequency is 50 kHz, the output voltage enters into steady state after 21 cycles. The voltage drop is 1 V in Fig. 10, 5.3% of nominal output while the voltage drop is 0.9 V in Fig. 11, 4.7% of the nominal output.

In order to check whether the sensed voltage for PSS is correct or not when the load changes from 20% to 100%, the sensed voltage in the DSP chip is transmitted to a digital-to-analog converter immediately after the A/D conversion and scaled to the same level of the output voltage. The results are shown in Fig. 12(a). Because we sense the output voltage from the auxiliary winding, the output voltage after the LC filter can not be obtained for voltage regulation. This phenomenon is obviously shown in Fig. 12(a), where the sensed voltage follows the output voltage before the LC filter. Figure 12(b) is the relation of the output voltage before the LC filter versus the sensed voltage. According to

V. CONCLUSION

PSS technique gradually becomes the solution for low power applications. The sensing error caused by the winding resistance and the voltage drop of the secondary diode can be corrected by modulating the sampling instant. For controller design, the conventional model and design procedure of flyback converters are suitable for flyback converters with PSS technique. With the advance of power control IC realization technology, digital technique is able to implement more sophisticated control and protection to improve the performance of power systems. In this paper,
we verify that the PSS technique is applicable to flyback converters. The performance of voltage regulation is excellent with only 1% deviation. PSS technique only controls the output voltage before the LC filter, which means that the output voltage after the LC filter is uncontrolled. Therefore, the LC filter must be designed properly to avoid unstable conditions or a large voltage drop when a load step change occurs.

REFERENCES


