A Novel Soft-Switching Full-Bridge Converter

Chia-Wei Lee and Ching-Shan Leu
Power Conversion Laboratory
Department of Electrical Engineering
National Taiwan University of Science and Technology
Taipei, Taiwan, R.O.C 106
cleu@mail.ntust.edu.tw

Abstract — Inserting an auxiliary switch to the conventional hard-switch full-bridge topology, a novel soft-switching full-bridge converter is proposed. Instead of the main switches, the auxiliary switch is pulse-width modulated to regulate the output voltage and soft-switching operation of the main switches can be easily achieved over full line and load ranges. Consequently, the reduced switching losses can be compensated for the auxiliary switch’s losses and its efficiency approximates to that of the phase-shift full-bridge converter. It makes the proposed converter to be an alternative approach for high frequency high efficiency power conversion applications. In addition to the circuit analysis and operation principle, a 100 kHz, 300-400 V input and a 12 V, 300 W output prototype is implemented to demonstrate its feasibility.

Index Terms—Full-Bridge DC-DC converter, soft-switching

I. INTRODUCTION

Full-bridge topology is widely used for the high frequency high power applications [1-5]. The conventional hard-switching full-bridge converter has simple control scheme but suffers from high switching loss. On the contrary, phase-shift full-bridge converter (PSFB) has to be modified to achieve zero-voltage switching (ZVS) operation over full line and load ranges.

To extend the line and load ranges to achieve ZVS operation of the main switches, a novel soft-switching full-bridge converter is proposed as shown in Fig. 1. A pulse-width modulated auxiliary switch is inserting between the DC source and the full-bridge power stage. With the help of the auxiliary switch, ZVS operation of the four main switches can be easily achieved over full line and load ranges. Consequently, the reduced switching losses can be compensated for the auxiliary switch’s losses and its efficiency approximates to that of the phase-shift full-bridge converter. It makes the proposed converter to be an alternative approach for high frequency high efficiency power conversion applications. In addition to the circuit analysis and operation principle, a 100 kHz, 300-400 V input and a 12 V, 300 W output prototype is implemented to demonstrate its feasibility.

II. ANALYSIS AND CIRCUIT OPERATION

The circuit diagram and the key waveforms of the proposed full-bridge converter are shown in Fig. 1 and Fig. 2, respectively. The primary side of the power stage consists of four main switches, Q1, Q2, Q3, and Q4, and one auxiliary switch, Q5, and a transformer, T1. The transformer comprises one primary winding and two secondary windings with n:1 turns ratio. The inductor, Lk, represents the leakage inductance of the transformer.

![Fig. 1. (a) Circuit diagram and (b) key waveforms of the proposed converter](image)

Under steady state operation, six operating stages exist within half of the switching cycle as shown in Figs. 2(a) to 2(f).

(a) Stage 1 [{t0-t1}]

Before t0, main switches Q1 and Q2 are turned on. At t0, auxiliary switch Q5 is turned on. Due to the turning on of the rectifier diodes, DRI and DR2, the transformer windings are shorted. Consequently, the input voltage applies to the
leakage inductance, \( L_k \), and the primary current, \( i_p \), is linearly increased to reflect the demand of the load current. This interval ends at \( t_1 \), the load current is fully supplied by \( D_{R1} \) and \( D_{R2} \) is turned off. The time interval, \( t_0-t_1 \), becomes the duty cycle loss between the primary and the secondary of the transformer. It will affect the load regulation resulting in reducing the converter efficiency.

(b) **Stage 2 [t_1-t_2]**

At \( t_1 \), the input voltage \( V_i \) applies to the transformer primary and magnetically couples to the secondary. \( D_{R2} \) is reversed biased and \( D_{R1} \) is forward biased to deliver the power to the output.

(c) **Stage 3 [t_2-t_3]**

At \( t_2 \), auxiliary switch \( Q_5 \) is turned off and \( i_p \) is decreased with a resonant fashion. \( V_{ab} \) will be decreased from \( V_i \) to zero. The voltage across the \( Q_5 \), \( V_{DS5} \), will be increased from zero to \( V_i \).

The voltage, \( V_{ab(t)} \) and current, \( i_{p(t)} \), can be derived as:

\[
V_{ab(t)} = (V_i - nV_o) \cos \omega_o t - Z_o I_{p(t)} \sin \omega_o t + nV_o \quad (1)
\]

\[
i_{p(t)} = \frac{V_i - nV_o}{Z_o} \sin \omega_o t + I_{p(t)} \cos \omega_o t \quad (2)
\]

Where, \( \omega_o = \frac{1}{\sqrt{3LC}} \), \( Z_o = \sqrt{\frac{L}{3C}} \), \( L_s = L_k + n^2L_j \), \( C = C_j = C_s = C_4 \).

(d) **Stage 4 [t_3-t_4]**

At \( t_3 \), \( V_{ab} \) drops to zero resulting in shorting the transformer primary winding and turning on the MOSFETs’ body diodes, \( D_2 \) and \( D_3 \). Consequently, \( i_p \) is circulated via both \( Q_1-D_2 \) and \( Q_4-D_2 \). Both \( D_{R1} \) and \( D_{R2} \) are turned on to freewheel the output current.

(e) **Stage 5 [t_4-t_5]**

At \( t_4 \), main switches \( Q_3 \) and \( Q_2 \) are ZVS turned-on. Besides the auxiliary switch, all the semiconductor switches are turned on during this short time interval.

(f) **Stage 6 [t_5-t_6]**

At \( t_5 \), main switches \( Q_1 \) and \( Q_4 \) are turned off. The primary current, \( i_p \), charges the parasitic capacitances, \( C_1 \) and \( C_4 \). \( V_{ab} \) will be decreased to \( -V_i \) and the voltage \( V_{DS5} \) will be decreased to zero.

The voltage, \( V_{ab(t)} \) and current, \( i_{p(t)} \), can be derived as:

\[
V_{ab(t)} = -Z_{o2} I_{p(t)} \sin \omega_{o2} t \quad (1)
\]

\[
i_{p(t)} = I_{p(t)} \cos \omega_{o2} t \quad (2)
\]

Where, \( \omega_{o2} = \frac{1}{\sqrt{3LC}} \), \( Z_o = \sqrt{\frac{L}{3C}} \), \( C = C_1 = C_4 = C_s \).

At \( t_6 \), \( Q_3 \) is turned on with ZVS operation and another half switch cycle begins.

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Fig. 3. Equivalent circuit for the different operation stages of the proposed converter.
From the above discussions, the unique timing of the gate drive signals plays an important role in the circuit operation. Two switching frequencies are employed; one for the auxiliary switch and another one for the four main switches. The former is a twice frequency than that of the latter. The auxiliary switch is pulse-width modulated to regulate the output voltage. On the other hand, the gate drive signals of the main switches are fixed push-pull type with a small overlapping conduction period. Consequently, the transition during $t_4-t_5$ time interval can be smoothly operated under steady state operation.

The ZVS operation of the main switches, $Q_1$, $Q_2$, $Q_3$, and $Q_4$ can be easily achieved due to the reflected load current.

However, the auxiliary switch introduces additional conduction and switching losses. To minimize the switching loss, the ZVS operation condition of the auxiliary switch is investigated.

During $t_5-t_6$ time interval, the equivalent circuit is simplified and shown in Fig. 4. It is assumed that the output capacitors $C_{os}$ of the all MOSFET have the same value.

$$\frac{1}{2} L_i i_{ps(i)}^2 \geq \frac{3}{2} C_{os} V_s$$

(5)

To assure the ZVS of $Q_5$ over a wider load range, an external inductor is suggested to add.

However, the increase the ZVS operating load range will be compensated with the duty cycle loss as the same characteristic as that of the phase-shift full-bridge converter.

III. EXPERIMENTAL RESULTS

A 300-400 V input, 12 V output-voltage and 300 W output power converter is implemented and tested. It operates at 100 KHz. The transformer has a 12:1:1 turns ratio with 17 uH leakage inductance. A 30 uH external inductor is added to achieve ZVS over a wider load range operations.

Figures 5(a) and 5(b) show the voltage waveforms of the main switches under low-line full load and high-line light load condition, respectively. Four main switches, $Q_1$-$Q_4$, are always operated with ZVS turned on to verify the soft-switching performance of the main switches over wider line and load conditions.

Figure 6 shows the drive and the voltage waveforms of the auxiliary switch $Q_5$. As mentioned before, the ZVS is strongly dependent on the load condition. For instance, operated at 300 V/18 A or 400 V/12 A operating conditions, ZVS operation can be obtained. ZVS will be lost under lighter load conditions.

Finally, efficiency comparison of the power stage between the phase shift full-bridge converter and the proposed full-bridge converter is made and plotted as shown in Fig. 7. The proposed full-bridge converter maximum efficiency $91\%$ occurs at low line 50% load condition. As mentioned before, the reduced switching losses are compensated for the auxiliary switch’s losses and its efficiency approximates to that of the phase-shift full-bridge converter.
IV. CONCLUSION

A novel soft-switching full-bridge converter is proposed. With the help of the auxiliary switch, ZVS of the main switches can be easily achieved over full line and load operating conditions. On the contrary, ZVS operation of the auxiliary switch can be obtained over a wider load range if an external inductor is added. Consequently, the reduced switching losses are compensated for the auxiliary switch’s losses and 91% efficiency maximum can be obtained approximate to that of the phase-shift full-bridge converter. It makes the proposed converter to be an alternative approach to improve the efficiency for the high input voltage high power applications.

REFERENCES